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In-growth Test for Monolithic 3D Integrated SRAM

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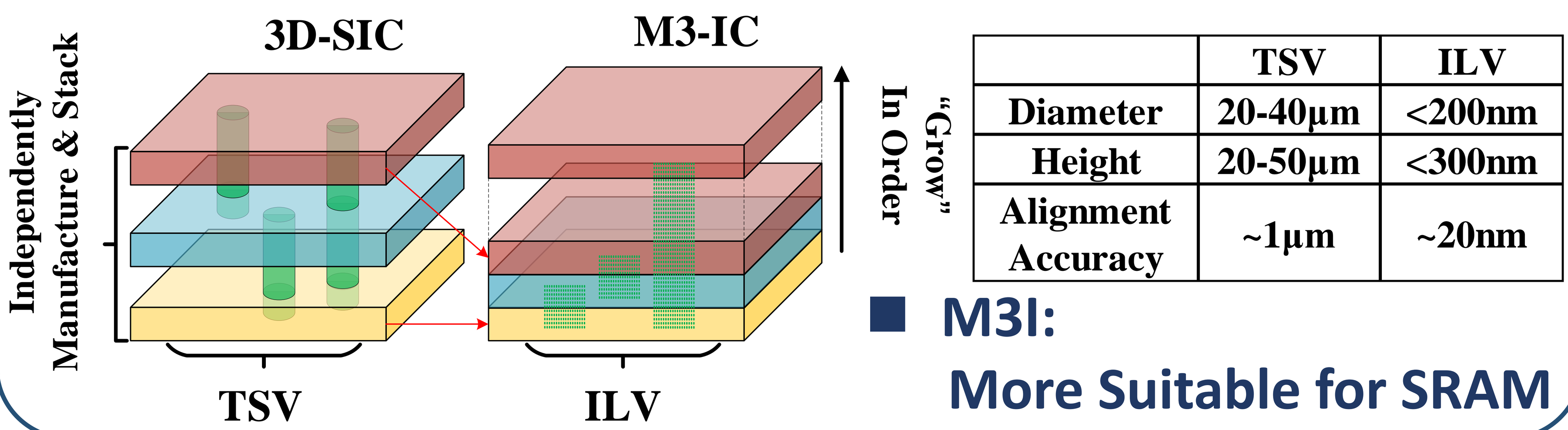
Advantages of Monolithic 3D Integration



	TSV	ILV
Diameter	20-40μm	<200nm
Height	20-50μm	<300nm
Alignment Accuracy	~1μm	~20nm

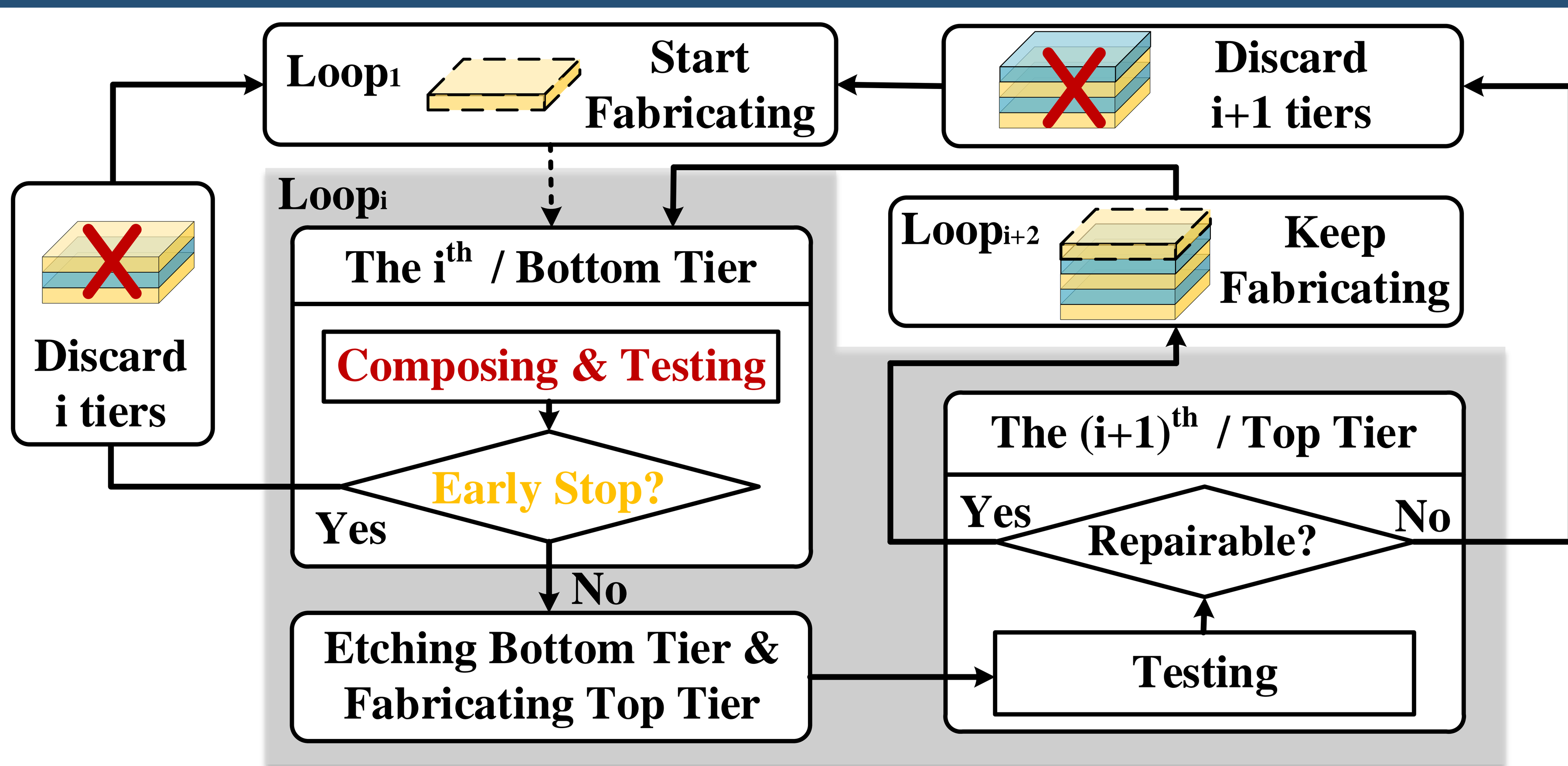
- M3I: More Suitable for SRAM

Challenge on Test Method of M3I SRAM

- **Testability Problem**
  - Incomplete circuit components and untestable
  - Unable to adding redundant transistors.
- **Reparability Problem**
  - Unable to repair a fault cell with a redundancy cell
  - Unknown reparability before fabrication finishes

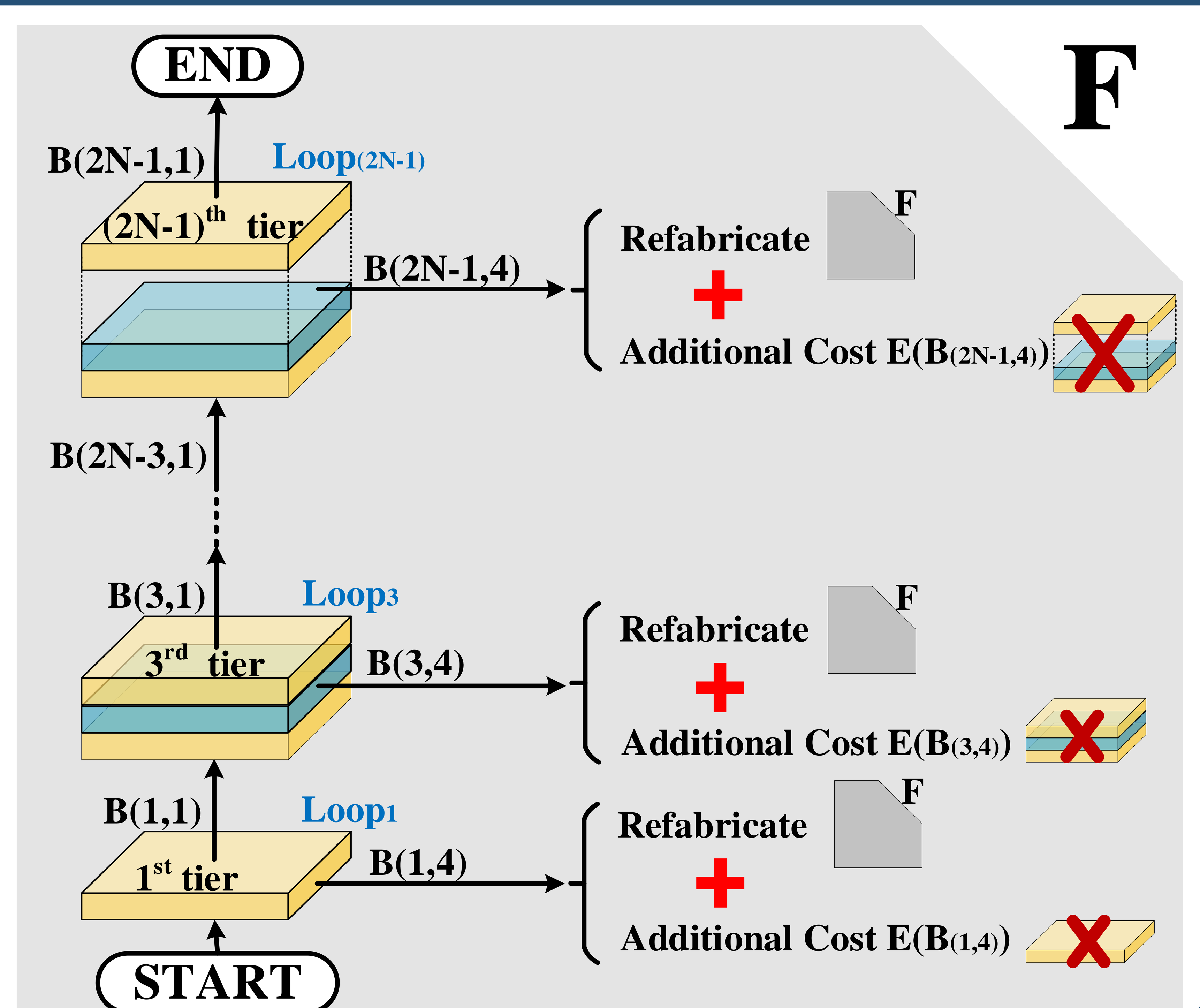
Lack of Efficient Pre-Bond Test Method & High Overall Fabrication Cost

Overview of Proposed Test Methodology

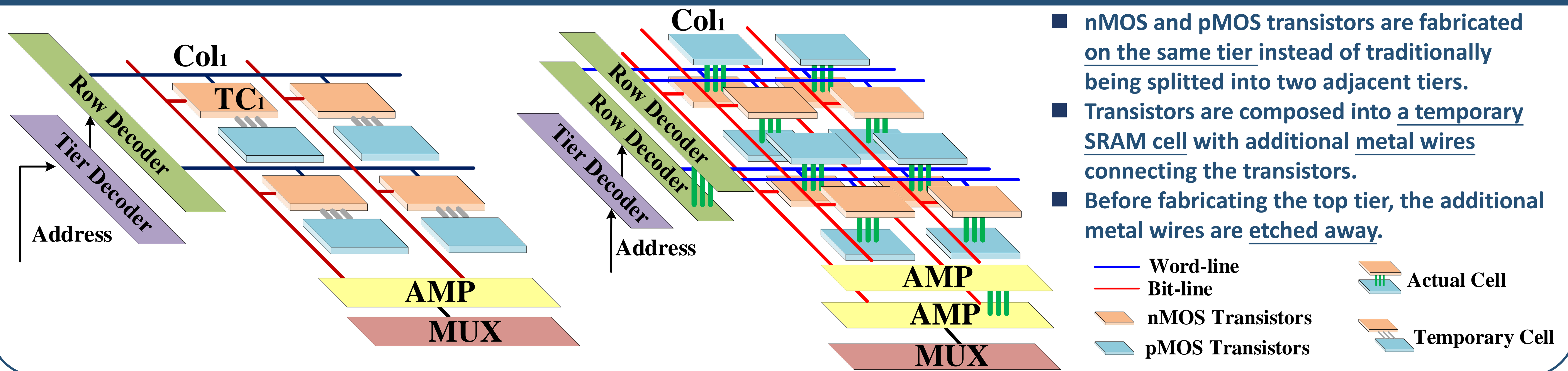


- **Composing & Testing**
  - A novel Design-for-Testability method enables the proposed In-growth test on cell-level partitioned incomplete SRAM cells.
- **Early Stop**
  - A judgement factor & a statistical cost model determine whether to stop the fabrication

Model of Cost to Guide Early Stop

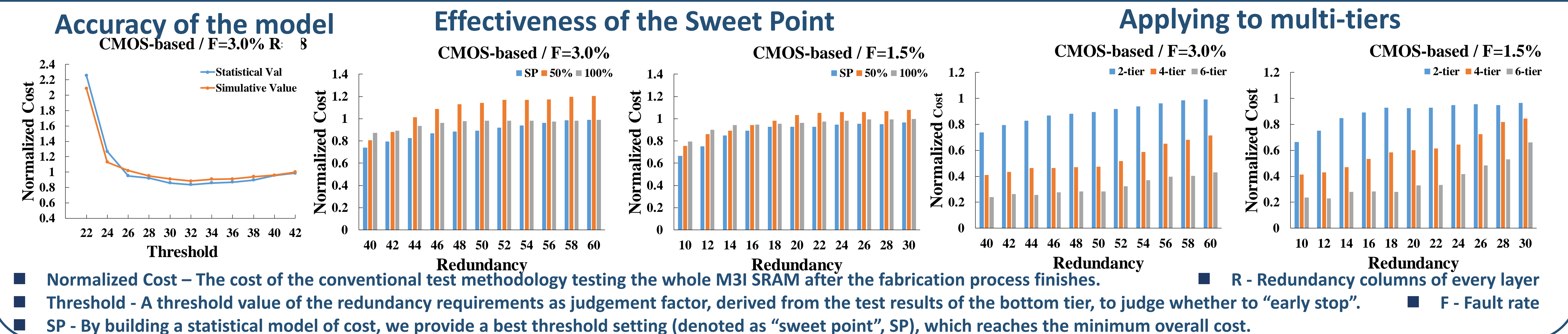


Design-for-Testability Method to Make Incomplete SRAM Cells Testable during Fabrication



- nMOS and pMOS transistors are fabricated on the same tier instead of traditionally being splitted into two adjacent tiers.
- Transistors are composed into a temporary SRAM cell with additional metal wires connecting the transistors.
- Before fabricating the top tier, the additional metal wires are etched away.

Experiment Results: The Effectiveness & The Better Performance with More Layers



- Normalized Cost – The cost of the conventional test methodology testing the whole M3I SRAM after the fabrication process finishes.
- R - Redundancy columns of every layer
- Threshold - A threshold value of the redundancy requirements as judgement factor, derived from the test results of the bottom tier, to judge whether to "early stop".
- F - Fault rate
- SP - By building a statistical model of cost, we provide a best threshold setting (denoted as "sweet point", SP), which reaches the minimum overall cost.